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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/652495
Filing Date: August 31, 2000
Appellant(s): AKRAM, SALMAN

Brick G. Power
For Appellant

EXAMINER'S ANSWER

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial prcceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Claims on Appeal

This appeal involves claims 1-3, 5-41 and 43-55.

(5) Status of Amendments After Final

No amendment after final has been filed.

(6) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(7) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection is correct.

(8) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Evidence Relied Upon

The following is a listing of the prior art of record relied upon in the rejection of the claims under appeal.

5,258,648	Lin	11-1993
5,229,647	Gnadinger	07-1993
6,004,867	Kim et al.	12-1999
6,294,405	Higgins, III	09-2001
5,870,289	Tokuda et al.	02-1999

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 112

(i) The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 11 recites the limitation "the another surface" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

(ii) The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5-9, 19-21, 22, 30-35, 43, 44 and 50-52, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Lin (US Pat. 5258648).

Regarding claim 1, 3, 5-9 and 19, Lin discloses a chip scale package (CSP)/flip chip composite package/flip chip carrier (FCC see 10 in Fig. 1-5) comprising:

- a semiconductor device/silicon chip (12 in Fig. 1) including an active surface having bond pads (14 in Fig. 1), the device being invertedly disposed on a first/top surface of a substrate/interposer (22 in Fig. 1-5)
- the substrate comprising a semiconductor material such as silicon (Col. 6, lines 30-40) having substantially the same coefficient of thermal expansion (CTE) as that of the device/chip, the device/chip and the substrate (12 and 22 respectively

in Fig. 1 and 3) having respective first and second thicknesses being substantially the same

- the substrate having electrically conductive traces (26 in Fig. 1) on a first surface, being disposed adjacent the active surface of the device and the substrate including a plurality of electrically conductive/filled vias on respective contact areas extending there-through (24 in Fig. 4; Col. 4, lines 52-65), the electrically conductive filled vias/material having one end being in electrical communication with/bonded to the conductive traces/contact areas and corresponding bond pads (Fig. 1-4) of the device, and
- electrically conductive solder balls/bumps (32 in Fig. 4; Col. 5, line 23) protruding from a second surface, the second surface being opposite to the first surface and the bumps being in electrical communication with respective electrically conductive vias

(Fig. 1-6; Col. 3, line 55- Col. 8, line 65).

Lin further discloses the substrate having conductive traces in communication of the vias, the traces being carried on/routed on the opposite surface/bottom surface extending in lateral directions from an end/second end of the conductive via of the plurality of the conductive vias (see traces 43/44 with respect to the solder balls/vias in Fig. 6; Col. 8, line 55-60; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

Regarding claims 21, 22 and 32-35, Lin discloses the entire claimed structure as applied to claim 1 above.

Regarding claims 43, 44 and 50-52, Lin discloses the entire claimed structure as applied to claim 1 above.

Claim Rejections - 35 USC § 103

(iii) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 11-14, 20, 23-25, 30, 31, 37-41 and 45-49, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Lin (US Pat. 5258648) in view of Gnadinger (US Pat. 5229647).

Regarding claim 2, Lin teaches substantially the entire claimed structure as applied to claim 1 above, except an electrically conductive bump protruding from the substrate opposite the semiconductor device, being in communication with the at least one electrically conductive via, and located at an opposite end of the at least one conductive trace from the at least one electrically conductive via.

Gnadinger teaches a multichip scale package comprising silicon substrate having a conventional via/bump configuration including electrically conductive/filled vias and protruding bump (see 21 and 20 respectively in Fig. 4) from a surface/bottom of the

substrate wherein the electrically conductive vias are plated with conventional metal plating/trace (see 28 in Fig. 4) such that the bump is in electrical communication with the electrically conductive via (Col. 3, line 35- Col. 4, line 35). Furthermore, the protruded bump is located at an opposite end/bottom of the electrically conductive metal plating/trace.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate electrically conductive bump protruding from the substrate opposite the semiconductor device, being in communication with the at least one electrically conductive via, and located at an opposite end of the at least one conductive trace from the at least one electrically conductive as taught by Gnadinger so that the via interconnect reliability can be improved in Lin's package.

Regarding claims 11-14, Lin teaches substantially the entire claimed structure as applied to claim 1 above, but fail to specify the second surface of the substrate being partially coated or substantially extended over with an insulating material.

Gnadinger teaches the multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, the insulating layer extending substantially over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second surface of the substrate being partially

coated or substantially extending over with an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin's package.

Regarding claim 20, Lin teaches substantially the entire claimed structure as applied to claim 1 above, except forming a diffusion region comprising a bond pad and via material.

Gnadinger teaches the multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Lin's package.

Regarding claims 23-25, Lin and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 21 and 20 above.

Regarding claims 30 and 31, Lin and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 21 and 2 above.

Regarding claims 37-41, Lin and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 21 and 11-14 above.

Regarding claims 45-49, Lin and Gnadinger teach substantially the entire claimed structure as applied to claims 1, 43 and 11-14 above.

(iv) Claims 10, 15, 18, 26, 27 and 36, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Pat. 5258648) in view of Kim et al. (US Pat. 6004867)

Regarding claim 10, Lin teaches substantially the entire claimed structure as applied to claim 1 above, except a first thickness of the semiconductor device being greater than that of the semiconductor substrate.

Kim et al. teach a CSP/FCC wherein a first thickness of the semiconductor device/chip (110 in Fig. 2) is greater than that of the semiconductor substrate (120 in Fig. 2).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate first thickness of the semiconductor device being greater than that of the semiconductor substrate as taught by Kim et al. so that manufacturing yield and processing/cycle time can be improved in Lin et al's package.

Regarding claims 15 and 18, Lin teaches substantially the entire claimed structure as applied to claim 1 above, except an intermediate layer being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Kim et al. teach the CSP/FCC comprising an intermediate/passivation layer (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate adhering the device and the substrate.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate intermediate layer being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer as taught by Kim et al. so that the surface protection can be improved in Lin's package.

Regarding claims 26 and 27, Lin and Kim et al. teach substantially the entire claimed structure as applied to claims 1, 21, 15 and 18 above.

Regarding claim 36, Lin and Kim et al. teach substantially the entire claimed structure as applied to claims 1, 21 and 10 above.

(v) Claims 16, 17, 28, 29, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Pat. 5258648) and Kim et al. (US Pat. 6004867) and as applied to claims 1, above, and further in view of Higgins, III (US Pat. 6294405).

Regarding claims 16 and 17, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, except the intermediate layer comprising an adhesive material or polyimide.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) adjacent a such as polyimide, silicon oxide, etc. (Col. 2, line 65) to provide a protection and bonding/adhesion for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising an adhesive material as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claims 28 and 29, Lin, Kim et al. and Higgins, III teach substantially the entire claimed structure as applied to claims 1, 21 and 16 and 17 above.

(vi) Claims 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Lin (US Pat. 5258648) in view of Tokuda et al. (US Pat. 5870289).

Regarding claims 53-55, Lin teaches substantially the entire claimed structure as applied to claims 1 and 43 above, except an adhesive layer disposed adjacent the first surface of the substrate.

Tokuda et al. teach a chip/substrate structure having through-holes/vias wherein a conventional adhesive layer/polyimide (see 30 in Fig. 1) is disposed adjacent/on a first/top surface of a wiring substrate (20 in Fig. 1) such that the through-holes/vias

extend through the adhesive layer to provide the desired electrical connection (see 40 in Fig. 1; Col. 10, line 30- Col. 11, line 10).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the polyimide/adhesive layer being disposed

adjacent the first surface of the substrate wherein one end of at least one end of the via extends through the adhesive layer as taught by Tokuda et al. so that the passivation/ surface protection for the substrate can be improved in Lin and Kim et al's package.

(11) Response to Argument

A. Rejection of independent claim 1 and dependent claims 3, 5-9 and 19 [Rejection under 35 U.S.C. 102(b)]:

Appellant argues that Lin does not expressly or inherently describe a CSP that includes conductive traces that communicate with conductive vias and that are carried upon a second surface of a substrate, which is opposite the surface adjacent to which a semiconductor device is positioned. Furthermore, the terminal groupings in Lin are not conductive traces; instead, they are solder balls or solder ball-like protrusions that are used to form multiple electrical connections.

Lin discloses the CSP/flip chip package comprising the substrate having a first surface adjacent the active surface of the device (see top surface of 22 in Fig. 4) and the substrate including a plurality of electrically conductive/filled vias extending there-

through (24 in Fig. 4; Col. 4, lines 52-65), the electrically conductive filled vias/material having one end on the first surface of the substrate being in electrical communication with/bonded to the bond pads (14 in Fig. 1-4) of the device. Lin further discloses the second/bottom surface of the substrate, which is opposite the first surface on which the semiconductor device is positioned, the second/bottom surface having terminal groupings/wiring in communication with respective vias (see 43/44 connecting respective vias in Fig. 6), the terminal groupings/wiring being carried on/routed on the second surface/bottom surface of the substrate extending in lateral directions from an end/second end of the conductive via of the plurality of the conductive vias (Fig. 4 and 6). Lin clearly discloses such terminal groupings/wiring being in a configuration/form of conductive traces to provide the desired routing including power/ground connections for the vias on the second surface opposite the surface on which the device is positioned (Col. 8, line 55-60; Col. 7, line 35-55).

Furthermore, such substrate/interposer configuration in Lin provides the conductive traces/wiring on both surfaces of the substrate including the first/top surface and the bottom/second surface (Col. 8, lines 52-60).

B. Rejection of independent claim 21 and dependent claims 22 and 30-35 [Rejection under 35 U.S.C. 102(b)]:

Appellant argues that Lin does not expressly or inherently describe that the terminal groupings being conductive traces on the second surface of the substrate and

the description of Lin is limited to the interposer with conductive traces that extend across the first surface of the substrate adjacent the device.

These arguments have been addressed above in the section A.

C. Rejection of independent claim 43 and dependent claims 44 and 50-52 [Rejection under 35 U.S.C. 102(b)]:

Appellants' arguments repeat Lin's lack of teaching to provide the conductive traces on the second surface of the substrate in the flip chip carrier.

These arguments have been addressed above in the section A.

D. Rejection of claims 2, 11-14, 20, 23-25, 30, 31, 37-41, and 45-49 [Rejection under 35 U.S.C. 103(a)]:

Appellant argues that the secondary reference of Gnadinger lacks any teaching or suggestion of substrate with conductive traces on the surface thereof that are to face away or be located opposite from the semiconductor device (e.g., the second surface of the substrate).

However, as addressed in the response in the section A above, the primary reference of Lin clearly discloses the substrate having conductive traces on the first/top and second/bottom surfaces.

E. Rejection of claims 10, 15, 18, 26, 27 and 36

[Rejection under 35 U.S.C. 103(a)]:

Appellant argues that the secondary reference of Kim et al. does not teach an interposer having with conductive traces on the exposed surface facing away from the semiconductor device.

However, as addressed in the response in the section A above, the primary reference of Lin clearly discloses the substrate having conductive traces on the first/top and second/bottom surfaces.

F. Rejection of claims 16, 17, 28 and 29

[Rejection under 35 U.S.C. 103(a)]:

Appellant argues that the secondary reference of Higgins, III lacks any teaching or suggestion of substrate having with conductive traces on the surface opposite the semiconductor device (e.g., the second surface of the substrate).

However, as addressed in the response in the section A above, the primary reference of Lin clearly discloses the substrate having conductive traces on the first/top and second/bottom surfaces.

G. Rejection of claims 53-55

[Rejection under 35 U.S.C. 103(a)]:

Appellant's arguments for the above rejection over Lin in view of Tokuda et al. have been addressed in the response in the section A above.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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July 20, 2006